II.   AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listings of claims.

1. (Currently Amended) A method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing ~~information~~ process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

defining technology ground rules and methodology constraints for each problem object;

individually determining a scaling factor for each problem object without considering a scale factor of a different problem object of the same type as the problem object;

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object.

2. (Previously Presented) The method of claim 1, wherein the at least two problem objects are selected from the group comprising: a layer, a region and a cell.

3. (Original) The method of claim 1, wherein the placement and routing performing step includes using an optimization-based hierarchical scaling program to produce a legal layout for each problem object.

4. (Original) The method of claim 1, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

5. (Previously Presented) The method of claim 1, wherein the identifying step includes:

    manufacturing the design layout;

    testing the manufactured design layout and identifying at least two problem objects that are problems; and

    generating the manufacturing information.

6. (Previously Presented) The method of claim 5, wherein the testing step includes characterizing operation and identifying the at least two problem objects by obtaining data indicating how well objects are able to be manufactured.

7. (Original) The method of claim 5, wherein the manufacturing information generating step includes generating the scaling target for the problem object.

8. (Original) The method of claim 1, further comprising the step of evaluating whether a new design layout including the scaled objects achieves an expected behavior.

9. (Currently Amended) A system for selectively scaling an integrated circuit design layout, the system comprising:

    means for identifying a scaling target for at least two problem objects of the design layout

based on <u>feedback from a</u> manufacturing ~~information~~ <u>process regarding problems caused by the</u> <u>problem objects in manufacturing an integrated circuit chip according to the design layout</u>;

means for defining technology ground rules and methodology constraints for each problem object;

means for <u>individually</u> determining a scaling factor for each problem object <u>without</u> <u>considering a scale factor of a different problem object of the same type as the problem object</u>;

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

means for, in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object.

10. (Original) The system of claim 9, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell.

11. (Original) The system of claim 9, wherein the placement and routing performing means includes means for conducting an optimization-based hierarchical scaling to produce a legal layout for each problem object.

12. (Original) The system of claim 9, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

13. (Previously Presented) The system of claim 9, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least two problem objects that are problems; and

means for generating the manufacturing information.

14. (Previously Presented) The system of claim 13, wherein the testing means includes means for characterizing operation and identifying the at least two problem objects by obtaining data indicating how well objects are able to be manufactured.

15. (Original) The system of claim 13, wherein the manufacturing information generating means includes means for generating the scaling target for the problem object.

16. (Original) The system of claim 13, further comprising means for evaluating whether a new design layout including the scaled objects achieves an expected behavior.

17. (Currently Amended) A computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout, the program product comprising:

program code, which when executed by a computer, configured to identify a scaling target for at least two problem objects of the design layout based on ~~feedback from a~~ manufacturing ~~information~~ process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

program code, which when executed by a computer, configured to define technology ground rules and methodology constraints for each problem object;

program code, which when executed by a computer, configured to <u>individually</u> determine

a scaling factor for each problem object <u>without considering a scale factor of a different problem</u>

<u>object of the same type as the problem object</u>;

program code, which when executed by a computer, configured to determine which at

least one of a plurality of scaling techniques is to be applied to each problem object, and scaling

each problem object with a respective at least one scaling technique and scaling factor; and

program code, which when executed by a computer, configured to, in the case that

assembly is required, perform placement and routing to assemble the design using the scaled

problem object.

18. (Original) The program product of claim 17, wherein the at least one problem object is

selected from the group comprising: a layer, a region and a cell.

19. (Original) The program product of claim 17, wherein the placement and routing performing

code includes program code configured to conduct an optimization-based hierarchical scaling to

produce a legal layout for each problem object.

20. (Original) The program product of claim 17, wherein the scaling factor is at least one of: a

compensation, a new ground rule and a scaling multiplier.

21. (Previously Presented) The program product of claim 17, wherein the identifying code

includes:

program code configured to test a manufactured design layout and identify at least two

problem objects that are problems; and

program code configured to generate the manufacturing information.

22. (Previously Presented) The program product of claim 21, wherein the testing code includes program code configured to characterize operation and identify the at least two problem objects by obtaining data indicating how well objects are able to be manufactured.

23. (Original) The program product of claim 17, wherein the manufacturing information generating code includes program code configured to generate a scaling target for the problem object.

24. (Original) The program product of claim 17, further comprising program code configured to evaluate whether a new design layout including the scaled objects achieves an expected behavior.

25-30. (Cancelled)

31. (Currently Amended) A method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing ~~information~~ process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

defining technology ground rules and methodology constraints for each problem object;

individually determining a scaling factor for each problem object <u>without considering a scale factor of a different problem object of the same type as the problem object</u>;

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object;

wherein the scaling factor includes at least one of a compensation and a new ground rule.

32. (Previously Presented) The method of claim 31, wherein the identifying step includes:

manufacturing the design layout;

testing the manufactured design layout and identifying at least two problem objects that are problems; and

generating the manufacturing information.

33. (Currently Amended) A system for selectively scaling an integrated circuit design layout, the system comprising:

means for identifying a scaling target for at least two problem objects of the design layout based on <u>feedback from a</u> manufacturing <s>information</s> <u>process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout</u>;

means for defining technology ground rules and methodology constraints for each problem object;

means for <u>individually</u> determining a scaling factor for each problem object <u>without</u>

considering a scale factor of a different problem object of the same type as the problem object;

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

means for, in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object;

wherein the scaling factor includes at least one of a compensation and a new ground rule.

34. (Previously Presented) The system of claim 33, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least two problem objects that are problems; and

means for generating the manufacturing information.

35. (Currently Amended) A computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout, the program product comprising:

program code, which when executed by a computer, configured to identify a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing ~~information~~ process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

program code, which when executed by a computer, configured to define technology ground rules and methodology constraints for each problem object;

program code, which when executed by a computer, configured to individually determine

a scaling factor for each problem object <u>without considering a scale factor of a different problem object of the same type as the problem object</u>;

program code, which when executed by a computer, configured to determine which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

program code, which when executed by a computer, configured to, in the case that assembly is required, perform placement and routing to assemble the design using the scaled problem object;

wherein the scaling factor includes at least one of a compensation and a new ground rule.

36. (Previously Presented) The program product of claim 35, wherein the identifying code includes:

program code configured to test a manufactured design layout and identify at least two problem objects that are problems; and

program code configured to generate the manufacturing information.